On the Optimum Width of GaAs MESFETs for Low Noise Amplifiers

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ABSTRACT

A derivation of the optimum device width for minimizing noise figure at a specified bias current is presented for a cascode LNA circuit topology in GaAs MESFET technology. This configuration achieves excellent third-order intercept and input return loss by employing source and series gate inductance. The resulting noise figure can be chosen close to F_{min} or traded for acceptable noise figure and/or input IP3 at reduced current consumption. Computer simulations confirm the predicted results.

It is generally known that GaAs MESFETs have superior noise figure and third-order input intercept compared to bipolar transistors. None-theless, few designs achieve noise figures close to the transistor F_{min}. To be sure, several factors prevent F_{min} from being attained in practice, but many designers employ an empirical, sometimes haphazard approach to implementing their circuits. While some assume that noise figure must be compromised to obtain a good input match, it has been shown that this is not the case [1],[2]. If a small input device is employed that requires a large input impedance transformation, the third-order input intercept can be degraded, sacrificing some of the inherent advantage of GaAs MESFETs unnecessarily. In this paper we develop a solution for the optimum device width of a GaAs MESFET to minimize noise figure at a specified bias current in a cascode LNA. Additionally, we investigate other trade-offs commonly encountered in practice.

Figure 1 is a simplified schematic diagram of a cascode amplifier with an input matching network consisting of source inductor L_s and series input inductor L_g. The output matching network is a traditional shunt L, series C arrangement. The real part of the input impedance can be made approximately equal to the generator impedance R_o with the proper selection of L_s, and the imaginary part can be made approximately equal to 0 by tuning-out C_{gs} with L_g [1],[2].

$$L_s \cong \frac{C_{gs}R_o}{g_m} \cong \frac{R_o}{2\pi f_t} \quad (1) \qquad L_g \cong \frac{1}{(2\pi f)^2 C_{gs}} - L_s \quad (2)$$

In [2] & [3] it is shown that the resulting noise figure with this choice is close to F_{min}. The corresponding value of v_{gs}, which is related to IIP_3, is

$$v_{gs} = \frac{v_{in}}{2}\frac{f_t}{f}\frac{1}{g_m R_o} \quad (3)$$

Typically, $g_m R_o \cong 2.5 \rightarrow 5$. f_t and g_m are the extrapolated short circuit current gain and transistor transconductance, respectively. It can be shown that the noise figure of this circuit at resonance is [2]

$$F \cong 1 + \frac{R_g + R_s + r_i}{R_o} + \Gamma g_m R_o \left(\frac{f}{f_t}\right)^2 \quad (5)$$

Here, R_g, R_s, and r_i are the gate, source, and input (in series with C_{gs}) extrinsic ohmic resistances of the FET, respectively. If the FET is implemented with parallel unit devices that are not very wide, say 30um or less, the gate resistance can be shown to be negligible, particularly with gold metalization. R_s and r_i vary inversely with total device width, W_T. Γ is a coefficient used to model channel noise for the FET, and typically varies from 2/3 (low field) to 3 depending on the FET

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and its bias condition. Unlike [2], we do not neglect R_s and r_i as their contribution to the noise figure in GaAs MESFET LNAs is substantial. f_t can be approximated with reasonable accuracy for low-to-moderate current density (usually chosen for LNAs) by

$$f_t \cong \frac{d(f_t)}{d(V_{gs}-V_t)}(V_{gs}-V_t) \equiv f_{t/v}(V_{gs}-V_t) \quad (5)$$

By using (4), (5) and

$$I_d \cong \beta W_T (V_{gs}-V_t)^2 \quad (6)$$

$$(V_{gs}-V_t) \cong \sqrt{\frac{I_d}{\beta W_T}} \quad (7)$$

$$g_m \cong 2\beta W_T (V_{gs}-V_t) \quad (8)$$

$$R_g + R_s + r_i \cong \frac{R_{ext}}{W_T} \quad (9)$$

one can show that

$$F \cong 1 + \frac{R_{ext}}{W_T R_o} + 2\beta\Gamma R_o \left(\frac{f}{f_{t/v}}\right)^2 \frac{W_T}{(V_{gs}-V_t)} \quad (10)$$

$$= 1 + \frac{R_{ext}}{W_T R_o} + 2\Gamma R_o \left(\frac{f}{f_{t/v}}\right)^2 \sqrt{\frac{\beta^3 W_T^3}{I_d}} \quad (11)$$

β is the FET transconductance parameter. Differentiating F with respect to W_T and equating it to 0 results in

$$W_T|_{opt} \cong \frac{f_{t/v}}{R_o f}\sqrt{\frac{R_{ext}(V_{gs}-V_t)}{2\beta\Gamma}} \quad (12)$$

$$\cong \left(\frac{f_{t/v}}{R_o f}\right)^{0.8} \frac{I_d^{0.2}}{\beta^{0.6}} \left(\frac{R_{ext}}{2\Gamma}\right)^{0.4} \quad (13)$$

$$F_{opt} \cong 1 + \frac{2f}{f_{t/v}}\sqrt{\frac{2\beta\Gamma R_{ext}}{V_{gs}-V_t}} \quad (14)$$

$$\cong 1 + \frac{2f}{f_{t/v}} \beta^{0.75} \left(\frac{W_T}{I_d}\right)^{0.25} (2\Gamma R_{ext})^{0.5} \quad (15)$$

$$\cong 1 + 2\left(\frac{f}{f_{t/v}}\right)^{0.8} \frac{(\beta R_{ext})^{0.6}}{(I_d R_o)^{0.2}} (2\Gamma)^{0.4} \quad (16)$$

Although Γ is generally bias dependent, we assume that a representative value can be employed when solving (13) and (16), or that the above equations can be solved iteratively if necessary knowing how Γ varies with bias. Γ is usually close to its minimum value for typically chosen current densities, minimizing this interaction.

Clearly, (11), (13), and (16) show that optimum noise figure is achieved when the contribution of channel noise is equal to that of the extrinsic ohmic resistances. Device width is increased (extrinsic resistance decreased) and f_t decreased (channel noise increased) until this is the case.

In practice, an LNA circuit will have a higher noise figure than a single transistor since other transistors, bias circuits, and matching networks with finite Qs will all degrade noise performance. The Q of L_g can be taken into account in (13) and (16) by substituting $R_{ext} + \frac{f_{t/v}}{2f\beta Q_{L_q}}$ for R_{ext}.

$$W_T|_{opt} \cong \left(\frac{f_{t/v}}{R_o f}\right)^{0.8} \frac{I_d^{0.2}}{\beta^{0.6}} \left(\frac{R_{ext} + \frac{f_{t/v}}{2f\beta Q_{L_g}}}{2\Gamma}\right)^{0.4} \quad (17)$$

$$F_{opt} \cong 1 + 2\left(\frac{f}{f_{t/v}}\right)^{0.8} \frac{\left(\beta\left[R_{ext} + \frac{f_{t/v}}{2f\beta Q_{L_g}}\right]\right)^{0.6}}{(I_d R_o)^{0.2}} (2\Gamma)^{0.4} \quad (18)$$

It can be shown that the total device width can be related to v_{gs} in the following way.

$$W_T \cong \frac{f_{t/v}}{f} \frac{1}{2R_o\beta} \frac{\frac{v_{in}}{2}}{v_{gs}} \quad (19)$$

(11) and (19) can be combined along with substituting $R_{ext} + \frac{f_{t/v}}{2f\beta Q_{L_q}}$ for R_{ext} to produce

$$F \cong 1 + \left(2\beta R_{ext}\frac{f}{f_{t/v}} + \frac{1}{Q_{L_g}}\right)\frac{v_{gs}}{\frac{v_{in}}{2}} + \Gamma\sqrt{\frac{f}{f_{t/v}}\frac{1}{2R_o I_d}\left(\frac{\frac{v_{in}}{2}}{v_{gs}}\right)^3} \quad (20)$$

(20) shows how noise figure varies with v_{gs}. This can be used to facilitate the trade-off of noise figure for IIP_3.

Figures 2 and 3 show optimum noise figure and FET width versus drain current for three values of Γ using R_o=50Ω, β=139μA/V^2, $f_{t/v}$=50GHz/V, and R_{ext}=800Ω-μm. Figure 4 shows a SPICE simulation of S11 and noise figure for a single FET, which agrees substantially with the presented results. Figures 5-7 show noise figure versus device width at 5mA for different frequencies and input inductor Q's. Figures 8 and 9 show noise figure versus v_{gs} for different values of Γ and drain current. Figure 10 shows how W_T varies with v_{gs}. Typically, the optimum device width is 1mm or more, resulting in a low value of R_n and v_{gs}.

References

[1] E. Heaney, F. McGrath, P.O. Sullivan, and C. Kermarrec, "Ultra Low Noise Amplifiers for Wireless Communications," *Proceedings of the GaAs IC Symposium*, 1993, pp. 49-51.

[2] D. Shaeffer & T. Lee, "A 1.5V, 1.5GHz CMOS Low Noise Amplifier," IEEE Journal of Solid-State Circuits, vol. 32, No. 5, May 1997, pp. 745-759.

[3] L. Boglione, R. Pollard, & V. Postoyalko, "The Pospieszalski Noise Model and the Imaginary Part of the Optimum Noise Source Impedance of Extrinsic or Packaged FETs," IEEE Microwave and Guided Wave Letters, vol. 7, No. 9, September 1997, pp. 270-272.

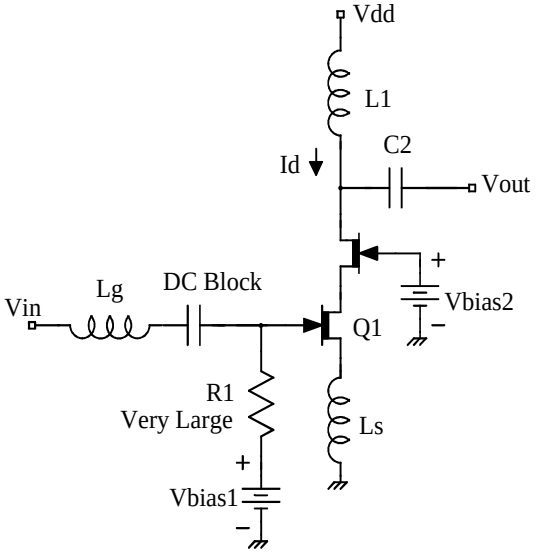

Figure 1. Simplified LNA Schematic Diagram.

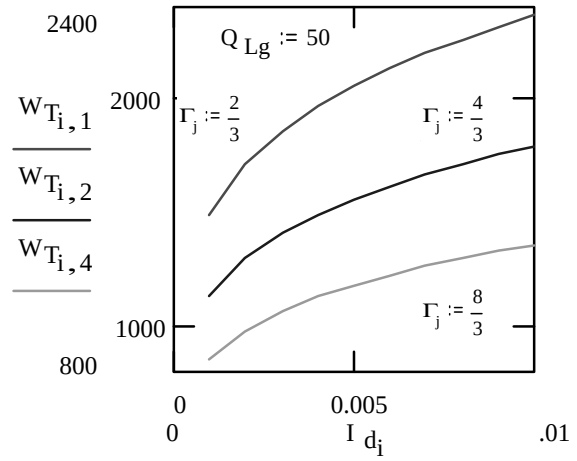

Figure 2. W_T vs Drain Current for F_{opt}, 900MHz.

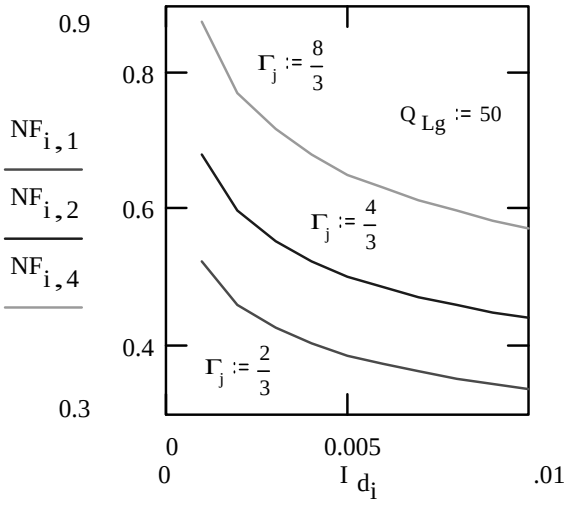

Figure 3. NF_{opt} (dB) vs Drain Current, 900MHz

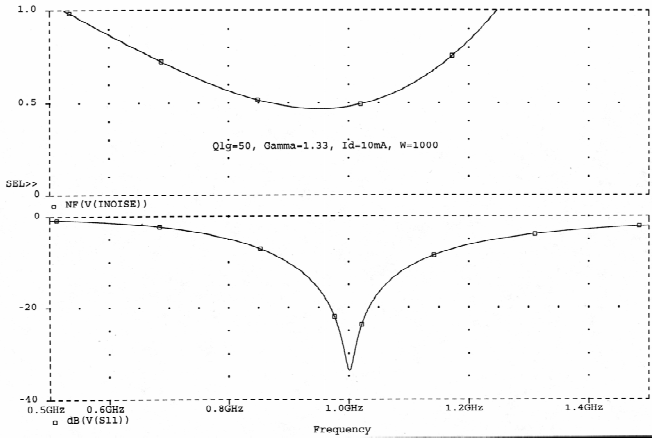

Figure 4. Simulated S11, Noise Figure, W=1000.

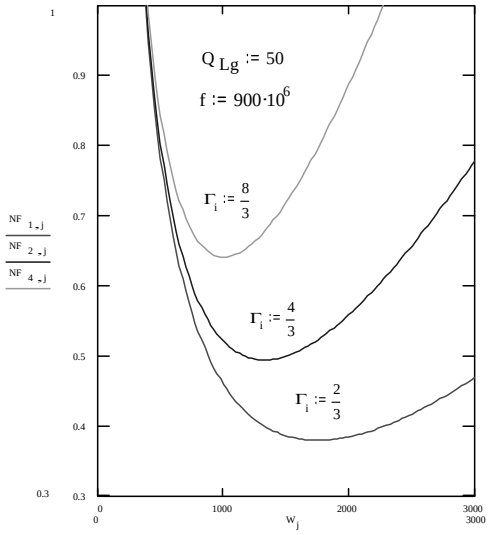

Figure 5. NF vs W_T, 5mA, 900MHz.

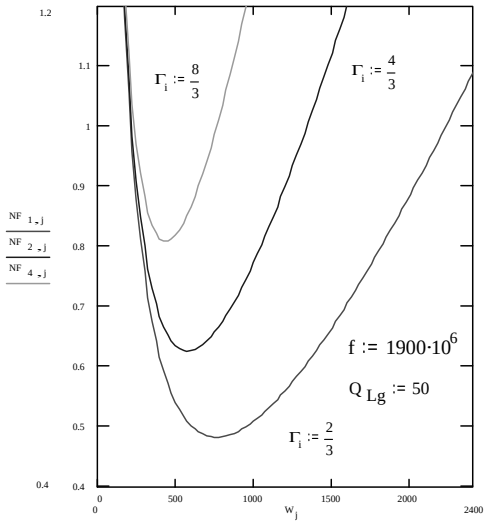

Figure 6. NF vs W_T, 5mA, 1900MHz, Q_{Lg}=50.

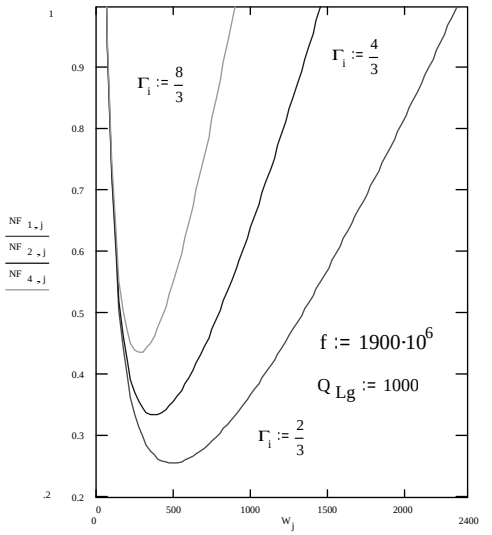

Figure 7. NF vs W_T, 5mA, 1900MHz, Q_{Lg}=1000.

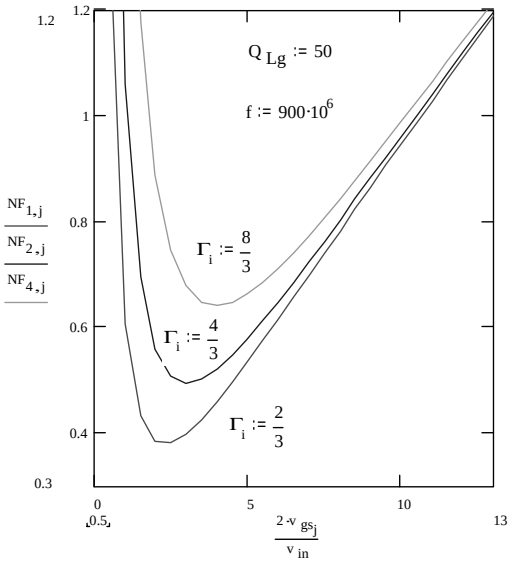

Figure 8. NF vs $2v_{gs}/v_{in}$ at 5mA.

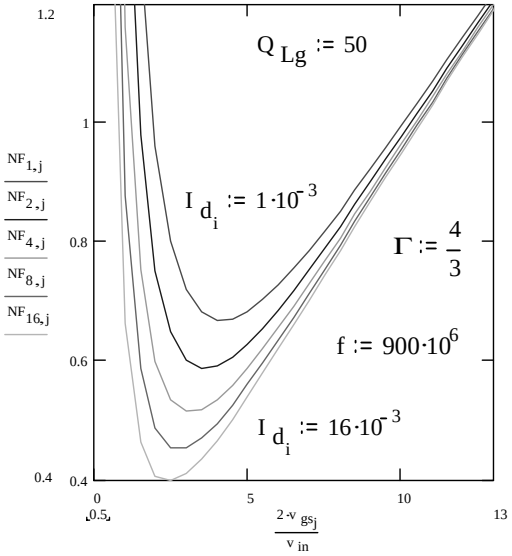

Figure 9. NF vs $2v_{gs}/v_{in}$, I_d.

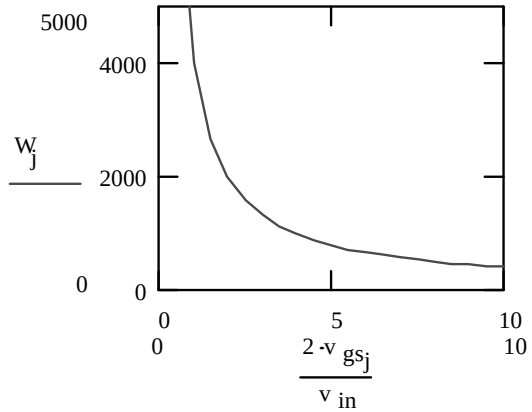

Figure 10. FET Width vs $2v_{gs}/v_{in}$.